SAVEETHA ENGINEERING COLLEGE
AUTONOMOUS
AFFILIATED TO ANNA UNIVERSITY

AI FIRST CAMPUS
Think AI. Live AI. Lead AI.

25 YEARS
OF EXCELLENCE

Centre of Excellence in

VLSI CHIP DESIGN

- Learn
- Innovate
- Design
- Verify
- Implement
- Lead



DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Skill-based, industry-aligned learning in VLSI, from RTL design to silicon-ready layouts and working FPGA hardware.

C2S
Selected under the Chip to Startup programme, MeitY

7
Industry EDA tool suites in the VLSI lab

4
FPGA platforms for hardware prototyping

₹7.5L
National-Level Digital Design Hackathon prize

Introduction

Building India's next generation of chip designers

The Centre of Excellence in VLSI Chip Design, in the Department of Electronics and Communication Engineering, gives students a strong foundation in VLSI and embedded systems. Learning is skill-based and industry-aligned, built on projects, hackathons and research, and guided by faculty with expertise in core technical domains.

C2S CHIP TO STARTUP

The institute is selected under the Government of India's Chip to Startup programme and approved to access Synopsys EDA tools for digital, analog and physical design. That access strengthens semiconductor education, research and student projects on campus.

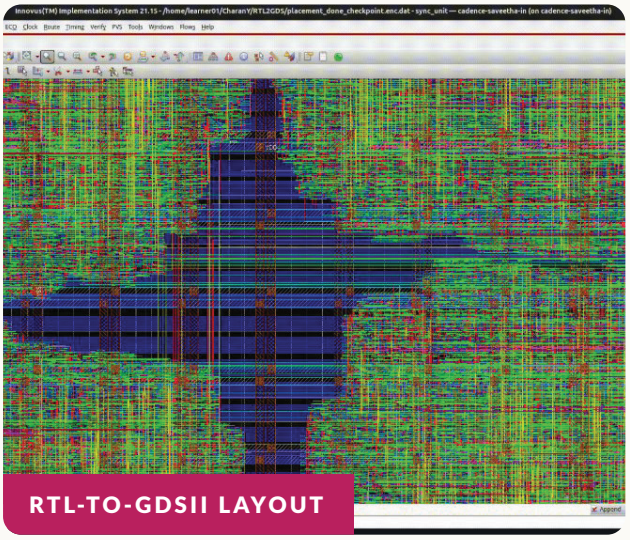
Area of work

Digital & RTL design
Verilog HDL and SystemVerilog, from micro-architecture through synthesis.

Design verification
SystemVerilog and UVM-based verification, with dedicated DV training for selected students.

Physical design & DFT
Complete RTL-to-GDSII flows, low-power techniques and design for testability.

FPGA prototyping
Real-time hardware validation on PYNQ-Z2, Spartan and Intel Cyclone boards.



RTL-TO-GDSII LAYOUT

FACILITIES

VLSI Design Laboratory

- 24 x 7 Wi-Fi Access for EDA Tools
- Industry-standard IC design environment for the complete RTL-to-GDSII flow
- Digital, analog, mixed-signal and physical design
- DFT, verification, low-power and signoff flows
- FPGA Development Boards

INDUSTRY EDA TOOLS

Cadence · Synopsys · Ansys · Keysight · Silvaco · Cadre · Compcarta

FPGA DEVELOPMENT BOARDS

- **PYNQ-Z2** FPGA board
- **Spartan-7** FPGA board
- **Spartan-6** Development kit
- **Intel Cyclone** FPGA board

Highlights

₹7.5 lakh

Prize won at the National-Level Digital Design Hackathon under the C2S programme (MeitY · C-DAC), March 2025

7 **Teams ranked**
NIT FPGA Hackathon, ranks 13

2 **Teams shortlisted of 500**
IESA DeepTech Hackathon with NXP Semiconductors

3 **Teams Participated**
DVCon India 2026 Design Contest

3 **Prize-winning finishes**
At national-level hackathons

Achievements

2nd runner-up
CHIP MONK Hackathon
Team RTL Architects

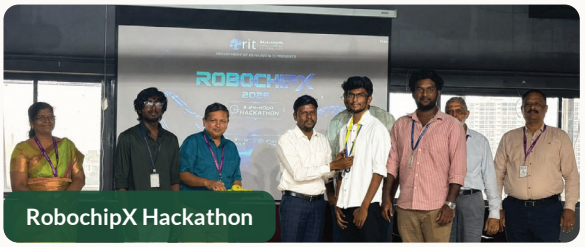
3rd prize
RobochipX Hackathon
Team Chip Makers

4 teams
Bharat AI-SoC Student Challenge
National participants · ARM & C2S, 2026



National-Level Digital Design Hackathon · ₹7.5 lakh prize


CHIP MONK Hackathon



RobochipX Hackathon

Industry internship achievements



Tonbo Imaging, Bengaluru
IMAGING & EMBEDDED VISION
Imaging, embedded vision and hardware systems for real-time defence-grade imaging.



Cadence Design Systems
PRODUCT VALIDATION ENGINEER · AMS
Analog/mixed-signal verification on the Cadence toolchain and an industry chip design flow.

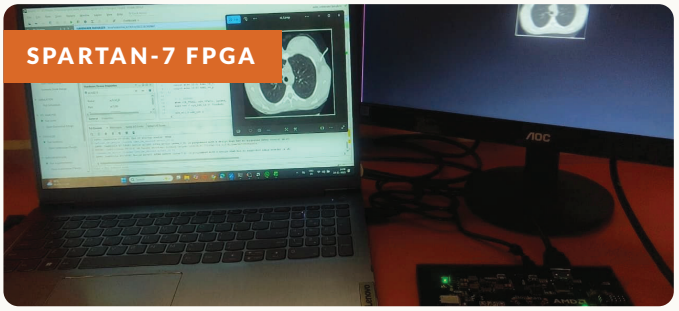
Projects & practical training

From real-time image processing to complete RTL-to-GDSII systems.



Real-Time Image Dehazing

A hardware-accelerated dehazing pipeline with custom HDL modules for feature extraction, transmission and reconstruction, removing haze from live video in real time.



FIR Filter for Medical Image Denoising

A separable linear-phase FIR filter for MRI/CT denoising, with a complete RTL pipeline and HDMI output for live image display.

Student projects

CAN-FD Controller on FPGA
CAN-FD and APB protocols, CDC architecture, timing closure and functional verification.

Low-Power ALU & Register File
Clock gating, operand isolation, activity monitoring and sleep-aware operation.

RISC-V Soft-Core SoC
RV32I SoC with complete RTL-to-GDSII implementation, validated on FPGA.

Multi-Clock FIFO ASIC
Synthesis, floorplanning, routing, timing analysis and GDSII generation.

RISC-V ADAS Zonal Controller
PicoRV32 SoC with AI accelerator and functional-safety unit, taken RTL-to-GDSII.

Real-Time Image Enhancement
AXI4-Stream processing pipeline on PYNQ-Z2 with HDMI output.

MIPI DSI Verification IP
UVM-based protocol VIP with reusable verification components.

AI Video-Processing SoC
On-device image enhancement and camera analytics for edge cameras.

Training path

01 Digital electronics
CMOS fundamentals

02 Verilog HDL
RTL & simulation

03 SystemVerilog
Design & verification

04 Verification
UVM testbenches

05 Physical design
Place, route & DFT

06 FPGA & GDSII
Validation & signoff

TRAINING THAT CONNECTS DESIGN TO HARDWARE

RTL to GDSII, taught on the tools industry uses

A dedicated Design Verification programme, delivered by eDigim Technologies, prepares selected students for DV internships and core VLSI roles. FPGA prototyping workshops on Spartan-7 and PYNQ-Z2 boards let students build and validate digital systems on real hardware.

PROFESSIONAL MEMBERSHIPS

VLSI Society of India

IESA INDIA ELECTRONICS & SEMICONDUCTOR ASSOCIATION
Taking India to ESDM Leadership

Access to national VLSI events, training, workshops and industry experts.

SAVEETHA ENGINEERING COLLEGE
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Centre of Excellence in VLSI Chip Design · Department of ECE

Be the Best.